Abstracts

Advanced silicon IC interconnect technology and design: present trends and RF wireless implications

R.J. Gutmann. "Advanced silicon IC interconnect technology and design: present trends and RF wireless implications." 1999 Transactions on Microwave Theory and Techniques 47.6 (Jun. 1999, Part I [T-MTT]): 667-674.

Back-end-of-the-line (BEOL) trends in silicon integrated circuits (ICs) include fully planarized interconnect structures with six levels of nonlocal wiring, copper metallization for improved resistance and electromigration, dual damascene patterning for improved line definition and lower BEOL manufacturing cost, and low dielectric constant interlevel dielectrics for reduced line and coupling capacitance. Advanced IC design complexity is being alleviated by the use of intellectual property (IP) cores or macrocells, particularly for advanced application-specific ICs and system-on-a-chip (SOC) implementations. Virtual Design Environment software, developed for distributed design of advanced printed circuit board, will expand to the chip level as SOC designs incorporate IP cores and involve increasingly complex interconnect wiring design. These trends are summarized and synergistic front-end developments discussed and implications for RF wireless technologies are presented. A timetable for such technology and design trends is projected based upon the 1997 National Technology Roadmap for Semiconductors.

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